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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,267	01/20/2004	Geum-Jin Yun	2557-000206/US	6863

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EXAMINER	
PATEL, PARESH H	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,267	YUN ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-14 and 16-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-14,16-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 08/08/2006 have been fully considered but they are not persuasive.

At page10 of the Remarks, with respect to claims 1, 4, 8, 12 and 21-22, Applicant argues that Horisaki et al. has no suggestion or teaching of an integrated burn-in test nor teaching of a multiple kind of a semiconductor devices including at least one of NVM, DRAM, and SRAM. Examiner disagrees because test pattern program which automatically generate a test pattern program for semiconductor devices such as a DRAM, a SRAM, a FLASH or the like (see Abstract of Horisaki et al.) includes "integrated" burn-in test program and "at least one of NVM, DRAM, and SRAM" as claimed. Horisaki et al. also discloses a muti-chip package includes a semiconductor devices having at least two of NVM, DRAM, and SRAM.

2. At page 11, for claims 1, 14, 21 and 27, and about Tom reference, Applicant argues that nowhere in Section III does it discloses uploading an **integrated** burn-in test **program** because Section III only discloses that a burn-in test is conducted on a MCM. Applicant further argues that there is no suggestion or teaching that a burn-in test **program** is used. Examiner again disagrees because at section II Tom reference test and burn-in of MCM using IBM's ES/9000 mainframe computer and uses pseudo-random pattern generator which generates a test pattern for BIST of MCM, therefore "integrated" and "program" is disclosed by Tom reference. At page 12, Applicant argues

that Tom reference discloses CMOS chip. Tom reference fails to suggest or teach a multiple kinds of semiconductor devices including at least two of NVM, DRAM, and SRAM. Examiner disagrees because Tom reference does disclose MCM is a memory array cell (see Section VII).

3. For claims 5-7, 9-11, 13, 19, 23-26 and 28 Applicant relies on the same argument as for Horisaki et al. Examiner disagrees for the same reason.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-6, 8-13, 21-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art (fig. 2A-2B) in view of Horisaki et al. (JP 2001-155497).

Regarding claims 1 and 21, Applicant admitted prior art (hereinafter APA) discloses conducting a test on each of the multiple kinds of semiconductor devices including at least two of a non-volatile memory, a SRAM, and a DRAM. APA does not disclose uploading an integrated burn-in test program as further claimed. Horisaki et al. (hereafter Horisaki) in fig. 1 and at Abstract discloses uploading an integrated burn-in test program and conducting a test using burn-in equipment [1 or 4] as further claimed for at least two of a non-volatile memory, a SRAM, and a DRAM [see Abstract].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the APA with teaching and suggestion as taught by Horisaki, in order to test MCM of multiple kinds to provide automatic operation and advantages that Horisaki has to offer.

Regarding claim 4, Horisaki discloses the multi-chip package performs a memory function [e.g. SRAM].

Regarding claims 5 and 24, APA at fig. 2A-2B discloses the test is conducted for each semiconductor device of the multi-chip package at a different temperature or a specific temperature.

Regarding claim 6, APA discloses a burn-in board and the chamber of burn-in equipment, as further claimed at paragraph 0008.

Regarding claims 8 and 22, Horisaki discloses the integrated burn-in test program uses a multiplexer selection function for applying a desired test condition [fig. 3 and paragraph 0005 and 0008] during testing of each semiconductor device.

Regarding claims 9 and 23, Horisaki is silent about the integrated burn-in test program has an I/O masking function for blocking some I/O terminals. Rather, at lines 7-10 of paragraph 0010, Horisaki discloses selection of number of I/O of semiconductor memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use test program as claimed to block I/O terminals, since test program with masking function as claimed is well known in the art for control application, particularly in code development program using address line.

Regarding claim 10, APA discloses the integrated burn-in test program has a function of setting a burn-in temperature condition for different kinds of semiconductor devices.

Regarding claims 11 and 25, APA discloses after loading the multi-chip package on the burn-in board to the chamber of the burn-in equipment, a contact test [step 11] is conducted to examine whether an electrical connection of the burn-in board is correct.

Regarding claim 12, Horisaki discloses the burn-in test is a monitoring burn-in test [using screen].

Regarding claims 13 and 26, APA discloses one time bean sorting, as further claimed.

Regarding claim 28, APA also discloses a chamber for its testing of multi-chip module during testing.

6. Claims 1, 14, 16-18, 20-21, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art (fig. 2A-2B) in view of Bardsley et al. (MCM BURN-IN EXPERIENCE).

Regarding claims 1, 14, 18 and 21, Applicant admitted prior art (hereinafter APA) discloses conducting a test on each of the multiple kinds of semiconductor devices including at least two of a non-volatile memory, a SRAM, and a DRAM. APA does not disclose uploading an integrated burn-in test program as further claimed.

Bardsley et al. (hereafter Tom) in fig. 1 discloses uploading a burn-in test program, conducting contact test on each of the semiconductor devices (different no. of

I/O pins) [chips and section III, memory array cell of Section VII], conducting sequentially [see fig. 1] a burn-in test [1st paragraph under section III] using test program [line 1 of section IV and stimulation, thermal control of section III] for each of the semiconductor devices and program controls the chamber temperature [section III and "Thermal Control" section of page 226, particularly 1st line of 3rd paragraph], ending the test and bin shorting [see fig. 1], as further claimed. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the APA with teaching and suggestion as taught by Tom, in order to test MCM of multiple kinds to provide cost effective operation and advantages that Tom has to offer.

Regarding claim 16, Tom discloses memory [CMOS tech. for memory cell].

Regarding claims 17 and 27, Tom discloses program for masking and blocking as further claimed using BIST and setting different temperature condition for each of the semiconductor devices [line 1 of 4th paragraph under "Thermal Control" section at page 226].

Regarding claim 20, Tom discloses monitoring burn-in test [see section "Thermal Control" at page 226].

Regarding claim 29, Tom discloses the burn-in board [the module substrate of section II] and a chamber ["module burn-in" of section III] of the burn-in equipment ["test equipment" of section III] as further claimed.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horisaki and APA, and further in view of Eide (US 6014316)

Regarding claim 7, Horisaki and APA is silent about the multi-chip package is in the form of a TBGA (thin ball grid array). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use TBGA, since it was known in the art that TBGA package also contains plurality of IC's or semiconductor devices for testing and packaging. Eide at fig. 7 and at lines 16-39 discloses TBGA to provide dense electronic package.

Regarding claim 19, Tom is silent about the multi-chip package is in the form of a TBGA (thin ball grid array). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use TBGA, since it was known in the art that TBGA package also contains plurality of IC's or semiconductor devices for testing and packaging. Eide at fig. 7 and at lines 16-39 discloses TBGA to provide dense electronic package.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 571-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paresh 10/30/06

Paresh Patel
Primary Examiner
Art Unit 2829

October 30, 2006